Benefits of Pipelining

Without Pipelining

	Clock Cycle														
	1					2					3				
Inst a	IF	ID	EX	MEM	WB										
Inst b						IF	ID	EX	MEM	WB					
Inst c											IF	ID	EX	MEM	WB

With Pipelining

	Clock Cycle														
	1	2	3	4	5	6	7								
Inst a	IF	ID	EX	MEM	WB										
Inst b		IF	ID	EX	MEM	WB									
Inst c			IF	ID	EX	MEM	WB								

Benefits of Branch Prediction

Without Branch Prediction

	1	2	3	4	5	6	7	8	9
Inst a	IF	ID	EX	MEM	WB				
BEQ n		IF	ID	EX	MEM	WB			
Inst c			IF	ID	EX	MEM	WB		
Inst d				IF	ID	EX	MEM	WB	
..									
Inst n					IF	ID	EX	MEM	WB

The comparison is not done until 3rd stage

These two instructions need to be removed from the pipeline

With Branch Prediction

	1	2	3	4	5	6	7		
Inst a	IF	ID	EX	MEM	WB				
BEQ n		IF	ID	EX	MEM	WB			
Inst c									
Inst d									
..									
Inst n			IF	ID	EX	MEM	WB		

If we predict that next instruction will be 'n'

Benefits of Forwarding

Without Forwarding

	1	2	3	4	5	6	7	8	9	10	11	12
LDR r1,A	IF	ID	EX	MEM	WB							
LDR r2,B		IF	ID	EX	MEM	WB						
ADD r3,r1,r2			IF	ID	Stall	Stall	EX	MEM	WB			
ST r3 C				IF	Stall	Stall	ID	Stall	Stall	EX	MEM	WB

With Forwarding

	1	2	3	4	5	6	7	8	9			
LDR r1,A	IF	ID	EX	MEM	WB							
LDR r2,B		IF	ID	EX	MEM	WB						
ADD r3,r1,r2			IF	ID	Stall	EX	MEM	WB				
ST r3 C				IF	Stall	ID	EX	MEM	WB			

Benefits of Superscalar

Scalar Processor

	1	2	3	4	5	6	7	8
ADD R0, R2, R3	IF	ID	EX	MEM	WB			
SUB R1, R4, R5		IF	ID	EX	MEM	WB		
MUL R0, R0, R1			IF	ID	EX	MEM	WB	
STR R0, x				IF	ID	EX	MEM	WB

Superscalar Processor

	1	2	3	4	5	6		
ADD R0, R2, R3	IF	ID	EX	MEM	WB			
SUB R1, R4, R5	IF	ID	EX	MEM	WB			
MUL R0, R0, R1		IF	ID	EX	MEM	WB		
STR R0, x		IF	ID	EX	MEM	WB		

In-order vs Scoreboard

In-order execution

	1	2	3	4	5	6	7	8	9	10	11	12	13
LD R0	I	RO	LD1	LD2	WB								
ADD R1, R0, R2		I	stall	stall	stall	RO	Add1	Add2	WB				
MUL R3,R2,R4						I	RO	Mul1	Mul2	Mul3	Mul4	WB	
DIV R7,R4,R5							I	RO	Div1	Div2	Div3	Div4	WB

Out of order with Scoreboard

	1	2	3	4	5	6	7	8	9	10
LD R0	I	RO	LD1	LD2	WB					
ADD R1, R0, R2		I	stall	stall	stall	RO	Add1	Add2	WB	
MUL R3,R2,R4			I	RO	Mul1	Mul2	Mul3	Mul4	WB	
DIV R7,R4,R5				I	RO	Div1	Div2	Div3	Div4	WB

These two instructions can overtake the stalled instruction

In-order vs Out-of-order

In-order

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
LD R1 X	I	RO	LD1	LD2	LD3	LD4	WB										
LD R2 Y		I	RO	LD1	LD2	LD3	LD4	WB									
ADD R3 R1 R2			I	Stall	Stall	Stall	Stall	Stall	RO	Add1	Add2	WB					
SUB R2 R5 R6									I	RO	Sub1	Sub2	WB				
MUL R4 R1 R1										I	RO	Mul1	Mul2	Mul3	Mul4	WB	
DIV R7 R5 R6											I	RO	Div1	Div2	Div3	Div4	WB

Out-of-order with Scoreboard

	1	2	3	4	5	6	7	8	9	10	11	12	13
LD R1 X	I	RO	LD1	LD2	LD3	LD4	WB						
LD R2 Y		I	RO	LD1	LD2	LD3	LD4	WB					
ADD R3 R1 R2			I	RO	RO	RO	RO	RO	Add1	Add2	WB		
SUB R2 R5 R6				I	RO	Sub1	Sub2	WB	WB	WB			
MUL R4 R1 R1					I	RO	RO	RO	Mul1	Mul2	Mul3	Mul4	WB
DIV R7 R5 R6						I	RO	Div1	Div2	Div3	Div4	WB	

Out-of-order with Tomasulo

	1	2	3	4	5	6	7	8	9	10	11
LD R1 X	I	LD1	LD2	LD3	LD4	WB					
LD R2 Y		I	LD1	LD2	LD3	LD4	WB				
ADD R3 R1 R2			I	RS	RS	RS	Add1	Add2	WB		
SUB R2 R5 R6				I	Sub1	Sub2	WB	WB	WB		
MUL R4 R1 R1						Mul1	Mul2	Mul3	Mul4	WB	
DIV R7 R5 R6						I	Div1	Div2	Div3	Div4	WB

Broadcast of results through the Bus allows not needing to wait for WB